REMARKS/ARGUMENTS

The Office Action mailed July 9, 2004, has been received and reviewed. Claims 1 through 12, and 36 through 40 are currently pending in the application. Claims 1 through 12, and 36 through 40 stand rejected. Applicants have amended claims 1, 12, and 36, entered new claims 45 through 48, and respectfully request reconsideration of the application as amended herein.

Preliminary Amendment

Applicants' undersigned attorney notes the filing herein of a Preliminary Amendment on November 30, 2001, which filing was not acknowledged in the outstanding Office Action. Should the Preliminary Amendment have failed for some reason to have been entered in the Office file, Applicants' undersigned attorney will be happy to have a true copy thereof hand-delivered to the Examiner.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,498,099 to McLellan et al. and U.S. Patent No. 6,700,188 to Lin

Claims 1 through 12, and 36 through 40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McLellan et al. (U.S. Patent No. 6,498,099 – hereinafter "McLellan '099") and Lin (U.S. Patent No. 670,188 – hereinafter "Lin"). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Applicants submit that claims 1 through 12 and 36 through 40 of the presently claimed invention are allowable over the references relied upon by the Examiner because the combined references fail to teach or suggest all of the limitations of the presently claimed invention.

Claims 1 through 11

Independent claim 1, as amended herein, is directed to a method of fabricating an integrated circuit package. The method comprises: providing a semiconductor die having a plurality of bond pads on an active surface thereof; providing a lead frame including a plurality of conductive leads; electrically coupling a first bond pad of the plurality of bond pads to a first portion of at least one conductive lead of the plurality of conductive leads; electrically coupling a second bond pad of the plurality of bond pads to a second portion of the at least one conductive lead; electrically isolating the first portion of the at least one conductive lead from the second portion of the at least one conductive lead; and *disposing a volume of electrically insulating material between the first portion of the at least one conductive lead and the second portion of the at least one conductive lead subsequent the electrically isolating the first portion from the second portion.*

The Examiner cites McLellan '099 as disclosing a method of fabricating an integrated circuit package, wherein the method comprises: "providing a semiconductor die 206 having a plurality of bonds on an active surface thereof; providing a lead frame 100 including a plurality of conductive leads 203, electrically coupling 205 a first bond of the plurality of bonds to a second portion of the at least one conductive lead; and electrically isolating the first portion of the at least one conductive lead from the second portion of the at least one conductive lead." (Office Action page 3). The Examiner cites Lin for the explicit disclosure of a plurality of bond pads on an active surface of the die and concludes that would have been obvious to combine the processes of McLellan '099 and Lin because it would facilitate wire-bonding. Applicants submit, however, that McLellan '099 and Lin fail to teach or suggest all of the limitations of claim 1 of the presently claimed invention.

McLellan '099 discloses a method of forming a leadless plastic chip carrier by half etching one or both sides of the package design or pattern onto a leadframe strip. Contact pads (203) are defined by the half etching process and then wire-bonded to a semiconductor die. The

leadframe (100) and semiconductor die (206) are molded within a plastic or epoxy material. Subsequent the molding operation, the leadframe is further etched to isolate the contact pads from other components of the leadframe. (See, e.g., col. 3, lines 9-56). However, McLellan '099 does not teach or suggest *disposing a volume of electrically insulating material between the first portion of the at least one conductive lead and the second portion of the at least one conductive lead subsequent the electrically isolating the first portion from the second portion*. Applicants further submit that Lin fails to teach or suggest such subject matter.

As such, Applicants submit that claim 1 is clearly allowable over the proposed combination of McLellan '099 and Lin. Applicants further submit that claims 2 through 11 are allowable at least be virtue of their dependency from an allowable base claim.

Applicants respectfully request reconsideration and allowance of claims 1 through 11.

Claim 12

Independent claim 12, as amended herein, is directed to a method of forming an array of electrically conductive elements on an integrated circuit package. The method comprises: securing a semiconductor die having a plurality of bond pads on an active surface thereof to a lead frame having a plurality of leads; electrically coupling at least two spaced locations of each lead of the plurality of leads with at least two different bond pads of the plurality of bond pads; severing each lead between the at least two spaced locations to form at least two electrically isolated conductive elements; and *disposing an electrically insulative material between the at least two spaced locations of each lead subsequent the severing.*

The Examiner cites McLellan '099 as teaching a method of forming an array of electrically conductive elements on an integrated circuit package wherein the method comprises: "securing a semiconductor die having a plurality of bonds on an active surface thereof to a lead frame having a plurality of leads; electrically coupling each lead of the plurality of leads at spaced locations with one of at least two different bonds of the plurality of bonds; and severing each lead between the spaced locations to form at least two electrically isolated conductive elements." (Office Action, pages 3 and 4). The Examiner cites Lin for the explicit disclosure of a plurality of bond pads on an active surface of the die and concludes that would have been obvious to combine the processes of McLellan '099 and Lin because it would facilitate wire-

bonding. Applicants submit, however, that McLellan '099 and Lin fail to teach or suggest all of the limitations of claim 12 of the presently claimed invention.

McLellan '099 discloses a method of forming a leadless plastic chip carrier by half etching one or both sides of the package design or pattern onto a leadframe strip. Contact pads (203) are defined by the half etching process and then wire-bonded to a semiconductor die. The leadframe (100) and semiconductor die (206) are molded within a plastic or epoxy material. Subsequent the molding operation, the leadframe is further etched to isolate the contact pads from other components of the leadframe. (See, e.g., col. 3, lines 9-56). However, McLellan '099 does not teach or suggest *disposing an electrically insulative material between the at least two spaced locations of each lead subsequent the severing.* Applicants further submit that Lin fails to teach or suggest such subject matter.

As such, Applicants submit that claim 12 is allowable over McLellan '099 and Lin and respectfully requests reconsideration and allowance thereof.

Claims 36 through 40

Independent claim 36, as amended herein, is directed to a method of fabricating a semiconductor die assembly. The method comprises: placing a semiconductor die within a plurality of leads extending laterally outwardly from peripheral edges thereof; wire bonding bond pads on the semiconductor die to spaced locations on each of the leads of the plurality; transfer molding a dielectric encapsulant over the semiconductor die, wire bonds and the plurality of leads, leaving undersurfaces of the plurality of leads exposed; severing each of the plurality of leads between the spaced locations; and *disposing a volume of electrically insulative material between the spaced locations subsequent severing each of the plurality of leads.*

The Examiner cites McLellan '099 as disclosing a method of fabricating a semiconductor die assembly wherein the method comprises: "placing a semiconductor die within a plurality of leads extending laterally outwardly form peripheral edges thereof; wire bonding bonds on the semiconductor die to spaced locations on the leads of the plurality; transfer molding a dielectric encapsulant over the semiconductor die, wire bonds and leads, leaving the undersurfaces of the lease exposed; and severing the leads between the spaced locations." (Office Action, page 5). The Examiner cites Lin for the explicit disclosure of a plurality of bond pads on an active surface

of the die and concludes that would have been obvious to combine the processes of McLellan '099 and Lin because it would facilitate wire-bonding. Applicants submit, however, that McLellan '099 and Lin fail to teach or suggest all of the limitations of claim 12 of the presently claimed invention.

As set forth hereinabove, McLellan '099 discloses a method of forming a leadless plastic chip carrier by half etching one or both sides of the package design or pattern onto a leadframe strip. Contact pads (203) are defined by the half etching process and then wire-bonded to a semiconductor die. The leadframe (100) and semiconductor die (206) are molded within a plastic or epoxy material. Subsequent the molding operation, the leadframe is further etched to isolate the contact pads from other components of the leadframe. (See, e.g., col. 3, lines 9-56). However, McLellan '099 does not teach or suggest *disposing a volume of electrically insulative material between the spaced locations subsequent severing each of the plurality of leads.* Applicants further submit that Lin fails to teach or suggest such subject matter.

As such, Applicants submit that claim 36 is clearly allowable over the proposed combination of McLellan '099 and Lin. Applicants further submit that claims 37 through 40 are allowable at least be virtue of their dependency from an allowable base claim.

Applicants respectfully request reconsideration and allowance of claims 36 through 40.

Obviousness Rejection Based on U.S. Patent No. 6,498,099 to McLellan et al. and U.S. Patent No. 6,700,188 to Lin et al., in combination with U.S. Patent No. 6,229,200 to McLellan et al.

As an initial matter, it is noted that claims 4 and 39 are stated to be rejected under 35 U.S.C. § 103(a) as being unpatentable over McLellan et al. (U.S. Patent No. 6,498,099) and Lin (U.S. Patent No. 670,188) as applied to claims 1 and 36, and "further in combination with McLellan et al. *(6372539)*." (Office Action, page 6, emphasis added). However, U.S. Patent 6,6372,539 is issued to Bayan (not McLellan) and does not appear to correlate with the cited references by the Examiner. Considering the citations set forth by the Examiner (i.e., col. 5, lines 13-15; and col. 6, line 60 to col. 7, line 9 of "McLellan") and the associated comments regarding such citations, it appears that the Examiner intended to rely on U.S. Patent No. 6,229,200 to McLellan. Applicants subsequent remarks presume the presently discussed rejection was

intended to be based on U.S. Patent 6,229,200 to McLellan (hereinafter "McLellan '200") rather than U.S. Patent No. 6,372,539 to Bayan.

Claim 4

Claim 4 depends from independent claim 1 and introduces the subject matter of mechanically severing the at least one conductive lead between the first portion and the second portion. The Examiner relies upon McLellan '099 and Lin as applied to claim 1 and then cites McLellan '200 as disclosing mechanical severing including making a linear cut between spaced locations. (See, Office Action, pages 6-7). The Examiner concludes that it would have been obvious to use or substitute the severing of McLellan '200 for at least some of the severing of McLellan '099 because it would provide severing, and use and substitution of a known element based on its suitability for its intended use has been held to be prima facie obvious. (See, Office Action page 7).

Applicants submit, however, that the references relied upon by the Examiner fail to teach or suggest all of the limitations of the presently claimed invention. As set forth hereinabove, McLellan '099 and Lin fail to teach or suggest *disposing a volume of electrically insulating material between the first portion of the at least one conductive lead and the second portion of the at least one conductive lead subsequent the electrically isolating the first portion from the second portion*. Applicants further submit that McLellan '200 fails to teach or suggest such subject matter.

As such, Applicants submit that claim 4 is allowable at least by virtue of its dependency from an allowable base claim and respectfully request reconsideration and allowance thereof.

Claim 39

Claim 39 depends from independent claim 36 and introduces the additional subject matter of the severing being effected by making a linear cut between the spaced locations on each lead. The Examiner relies upon McLellan '099 and Lin as applied to claim 1 and then cites McLellan '200 as disclosing mechanical severing including making a linear cut between spaced locations. (See, Office Action, pages 6-7). The Examiner concludes that it would have been obvious to use or substitute the severing of McLellan '200 for at least some of the severing of McLellan '099

because it would provide severing, and use and substitution of a known element based on its suitability for its intended use has been held to be prima facie obvious. (See, Office Action page 7).

Applicants submit, however, that the references relied upon by the Examiner fail to teach or suggest all of the limitations of the presently claimed invention. As set forth hereinabove, McLellan '099 and Lin fail to teach or suggest *disposing a volume of electrically insulative material between the spaced locations subsequent severing each of the plurality of leads*. Applicants further submit that McLellan '200 fails to teach or suggest such subject matter.

As such, Applicants submit that claim 4 is allowable at least by virtue of its dependency from an allowable base claim and respectfully request reconsideration and allowance thereof.

ENTRY OF AMENDMENTS

The amendments to claims 1, 12 and 36 and new claims 45 through 48 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1 through 12, 36 through 40 and 45 through 48 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,

Bradley B. Jensen
Registration No. 46,801
Attorney for Applicant(s)
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

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